

We claim:

1           1.       A method of preparing a pre-formed integrated circuit chip for  
2 encapsulation in an electronic package, comprising the steps of:  
3           forming an interconnect assembly separately from said pre-formed integrated  
4 circuit chip;  
5           forming a plurality of conductive bumps connected to the terminals of the  
6 integrated circuit chip;  
7           bonding said interconnect assembly to said prepared integrated circuit chip; and  
8           passivating said bonded interconnect assembly and said prepared integrated  
9 circuit chip into an integral structure to provide said electronic package.

1           2.       The method of claim 1 wherein said step of forming an interconnect  
2 assembly comprises forming said interconnect assembly on a releasable substrate.

1           3.       The method of claim 1 wherein said step of forming an interconnect  
2 assembly comprises forming at least one test pad in an interconnect layer, which at  
3 least one test pad can be accessed and electrically connected on opposing sides of  
4 said test pad.

1           4.       The method of claim 3 wherein said step of forming at least one test pad  
2 forms a test pad having gold on opposing sides of said test pad and sandwiched  
3 therebetween a conductive field metal.

4           5.       The method of claim 3 wherein said step of forming an interconnect  
5 assembly comprises forming at least one test pad in a plurality of stacked interconnect  
6 layers, each of which at least one test pad in each interconnect layer can be accessed  
7 and electrically connected on opposing sides of said test pad.

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4 said test pad, and wherein said step of bonding said interconnect assembly to said  
5 prepared integrated circuit chip flip bonds said solder layer onto one side of said test  
6 pad.

1 9. The method of claim 1 where said step of passivating said bonded  
2 interconnect assembly and said prepared integrated circuit chip into an integral  
3 structure to provide said electronic package comprises underfilling said prepared  
4 integrated circuit chip with an insulating material to remove all voids between said  
5 prepared integrated circuit chip and said interconnect assembly.

1 10. The method of claim 1 where said step of passivating said bonded  
2 interconnect assembly and said prepared integrated circuit chip into an integral  
3 structure to provide said electronic package comprises potting said interconnect  
4 assembly and said prepared integrated circuit chip into an integral package.

1 11. The method of claim 9 where said step of passivating said bonded  
2 interconnect assembly and said prepared integrated circuit chip into an integral  
3 structure to provide said electronic package comprises potting said interconnect  
4 assembly and said prepared integrated circuit chip into an integral package.

1 12. The method of claim 10 further comprising the step thinning said prepared  
2 integrated circuit chip.

1           13.    The method of claim 10 further comprising the step of accessing said  
2 prepared integrated circuit chip through electrical connection to said at least one test  
3 pad through a surface thereof opposing said surface of said test pad contacting a  
4 terminal of said prepared integrated circuit chip to test said prepared integrated circuit  
5 chip.

1           14.    The method of claim 10 wherein a plurality of interconnect assembly and  
2 prepared integrated circuit chips are bonded together to form a corresponding plurality  
3 of electronic packages and further comprising the step of releasing said plurality of  
4 electronic packages from each other.

1           15.    The method of claim 1 wherein a plurality of interconnect assembly and  
2 prepared integrated circuit chips are bonded together to form a corresponding plurality  
3 of electronic packages and further comprising the step of testing said interconnect  
4 assembly and bonding a tested interconnect assembly in said step of bonding said  
5 interconnect assembly to said prepared integrated circuit chip only if said interconnect  
6 assembly tested good.

1           16.    The method of claim 15 where said step of forming said plurality of  
2 interconnect assemblies comprises forming said interconnect assemblies  
3 simultaneously in a wafer and where said plurality of prepared integrated circuit chips  
4 are individually bump bonded to successfully tested ones of said interconnect  
5 assemblies.

1 17. An electronic package comprising:  
2 a pre-formed integrated circuit chip;  
3 an interconnect assembly separately from said pre-formed integrated circuit chip;  
4 a plurality of conductive bumps connected to the terminals of the integrated  
5 circuit chip, said interconnect assembly bonded to said prepared integrated circuit chip;  
6 and  
7 a passivating layer disposed about said interconnect assembly and said  
8 prepared integrated circuit chip after said interconnect assembly and said prepared  
9 integrated circuit chip have been bonded together thereby forming into an integral  
10 structure.

1 18. The electronic package of claim 17 wherein said interconnect assembly  
2 comprises is formed on a releasable substrate.

1 19. The electronic package of claim 1 wherein said interconnect assembly  
2 comprises at least one test pad in an interconnect layer, which at least one test pad can  
3 be accessed and electrically connected on opposing sides of said test pad.

1 20. The electronic package of claim 19 wherein said at least one test pad  
2 forms a test pad has gold on opposing sides of said test pad and sandwiched  
3 therebetween a conductive field metal.

4           21.    The electronic package of claim 19 wherein said interconnect assembly  
5 comprises a plurality of stacked interconnect layers and at least one test pad in said  
6 plurality of stacked interconnect layers, each of which at least one test pad in each  
7 interconnect layer can be accessed and electrically connected on opposing sides of  
8 said test pad.

1           22.    The electronic package of claim 21 wherein said at least one test pad in  
2 said plurality of stacked interconnect layers forms at least one test pad in each layer  
3 having gold on opposing sides of said test pad and sandwiched therebetween a  
4 conductive field metal.

1           23.    The electronic package of claim 17 where said plurality of conductive  
2 bumps are connected to terminals of the integrated circuit chip in order to make a  
3 connection to said terminals on said integrated circuit chip and further comprising a  
4 solder layer disposed on said conductive bump.

1           24.    The electronic package of claim 23 wherein said interconnect assembly  
2 comprises at least one test pad in said interconnect layer, which at least one test pad  
3 can be accessed and electrically connected on opposing sides of said test pad, and  
4 wherein said interconnect assembly is bonded to said prepared integrated circuit chip  
5 by a flip bond to said solder layer onto one side of said test pad.

1           25.    The electronic package of claim 17 where said passivating layer combines  
2   said interconnect assembly and said prepared integrated circuit chip into an integral  
3   structure and includes insulating material underfilling of said prepared integrated circuit  
4   chip to remove all voids between said prepared integrated circuit chip and said  
5   interconnect assembly.

1           26.    The electronic package of claim 17 where said passivating layer combines  
2   said interconnect assembly and said prepared integrated circuit chip into an integral  
3   structure and is comprised of a potting material.

1           27.    The electronic package of claim 25 where said passivating layer combines  
2   said interconnect assembly and said prepared integrated circuit chip into an integral  
3   structure and is comprised of a potting material.

1           28.    The electronic package of claim 26 where said prepared integrated circuit  
2   chip is thinned after being potted.

1           29.    The electronic package of claim 27 said prepared integrated circuit chip is  
2   accessed through electrical connection to said at least one test pad through a surface  
3   thereof opposing said surface of said test pad contacting a terminal of said prepared  
4   integrated circuit chip to test said prepared integrated circuit chip.

1           30.    The electronic package of claim 27 wherein a plurality of interconnect  
2 assembly and prepared integrated circuit chips are bonded together to form a  
3 corresponding plurality of electronic packages which are later released from each other.

1           31.    The electronic package of claim 17 wherein a plurality of interconnect  
2 assembly and prepared integrated circuit chips are bonded together to form a  
3 corresponding plurality of electronic packages in which said interconnect assemblies  
4 are tested and a tested interconnect assembly is bonded to said prepared integrated  
5 circuit chip only if said interconnect assembly tested good.

1           32.    The electronic package of claim 31 where in said plurality of interconnect  
2 assemblies said interconnect assemblies are formed simultaneously in a wafer and  
3 where said plurality of prepared integrated circuit chips are individually bumped bonded  
4 to successfully tested ones of said interconnect assemblies.

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